

FIG. 1

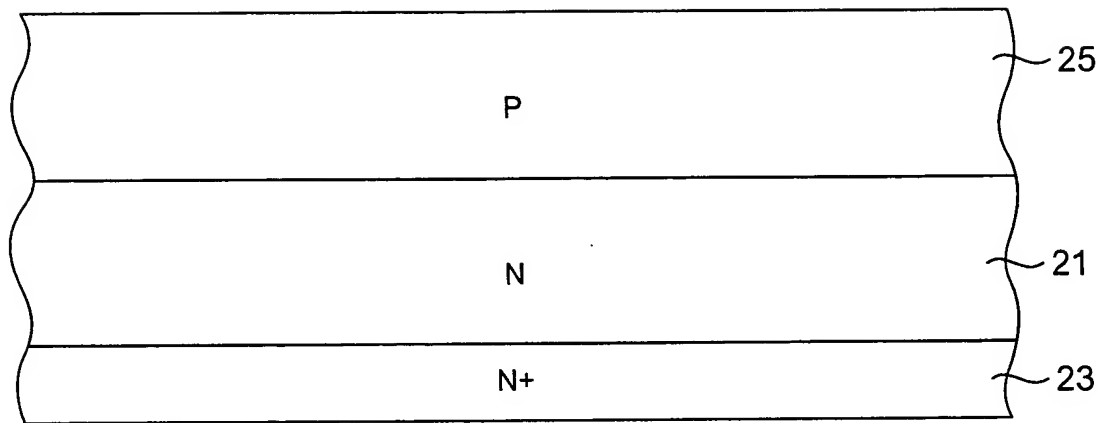


FIG. 2A

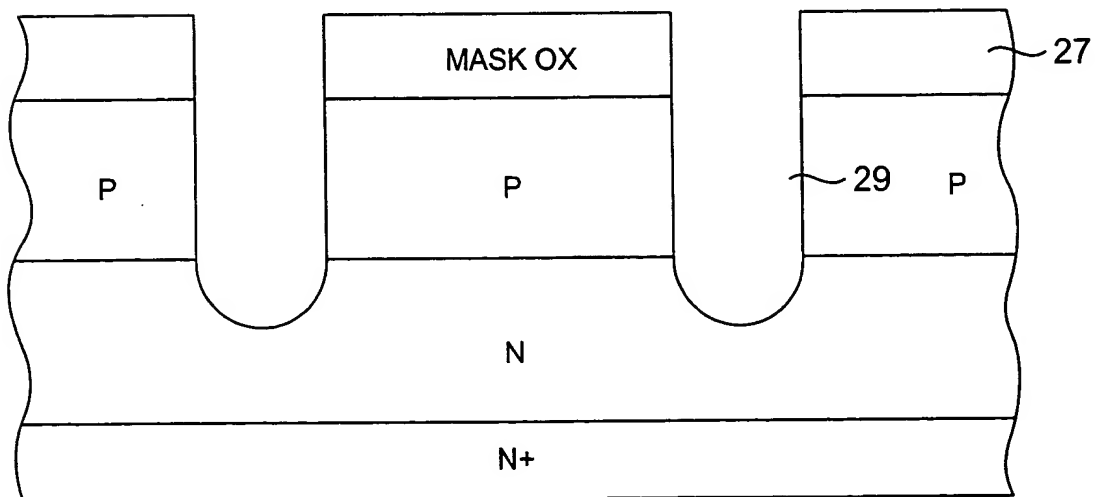


FIG. 2B

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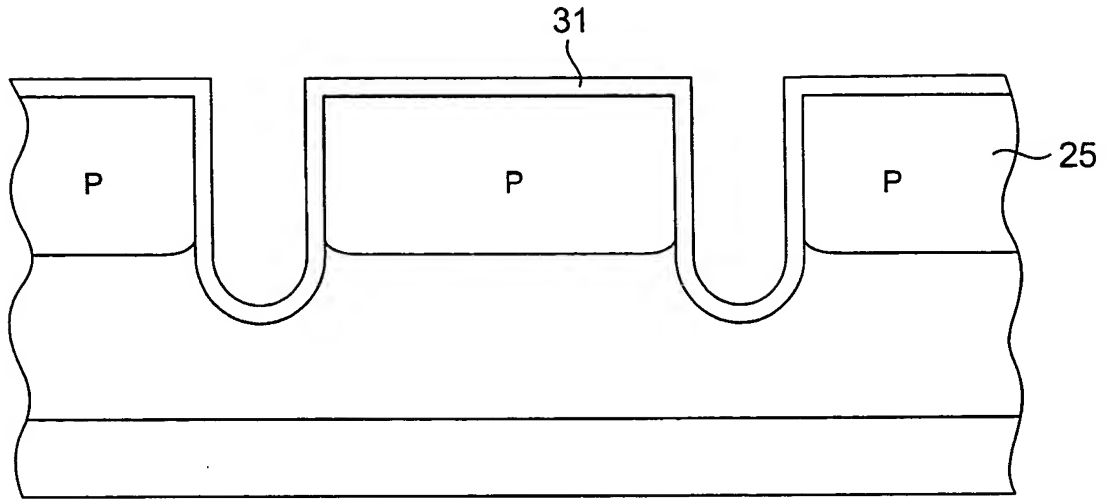


FIG. 2C

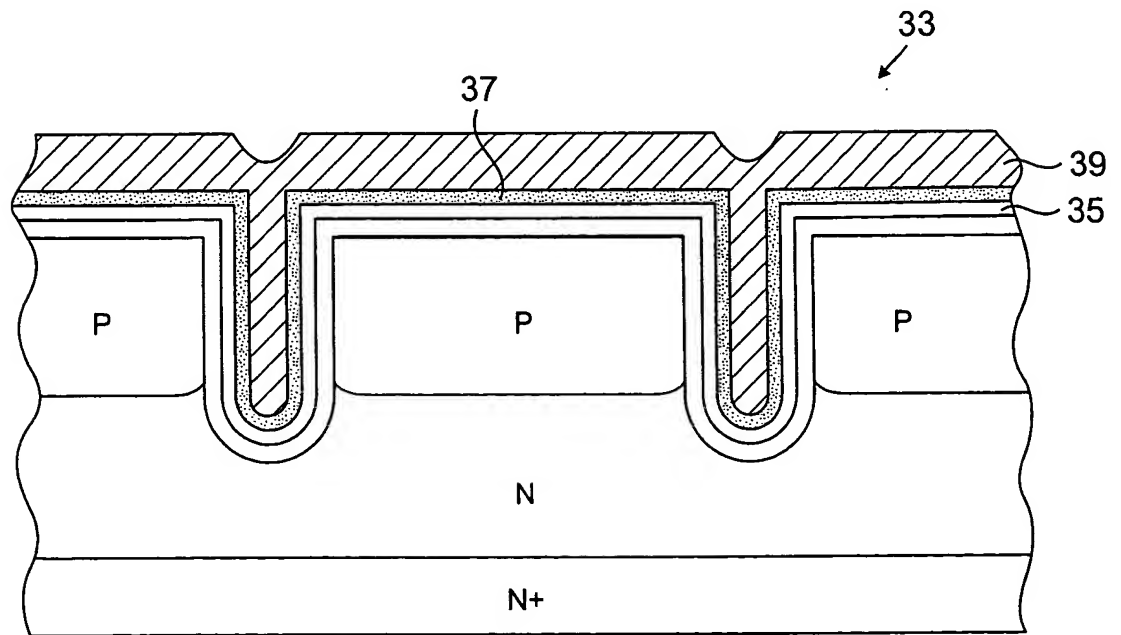


FIG. 2D

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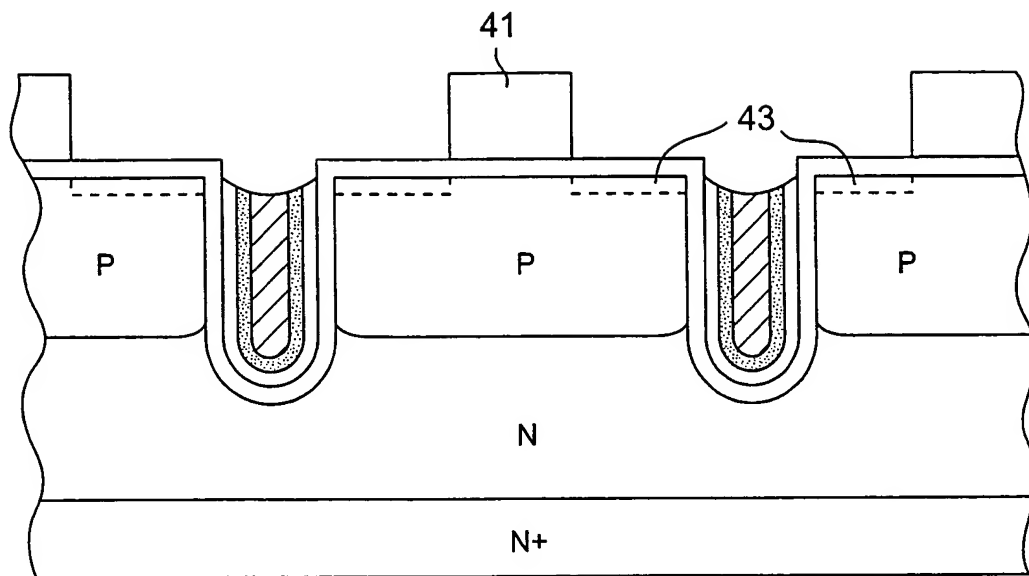


FIG. 2E

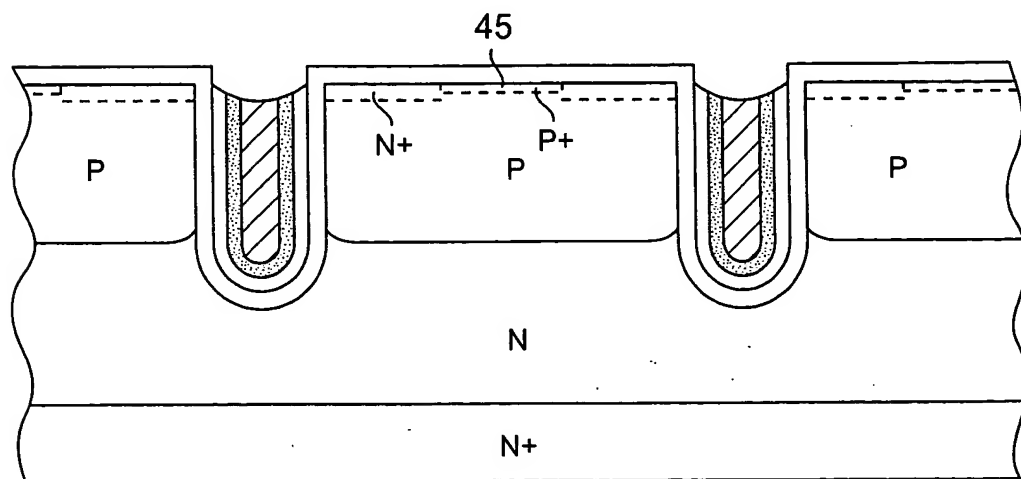


FIG. 2F

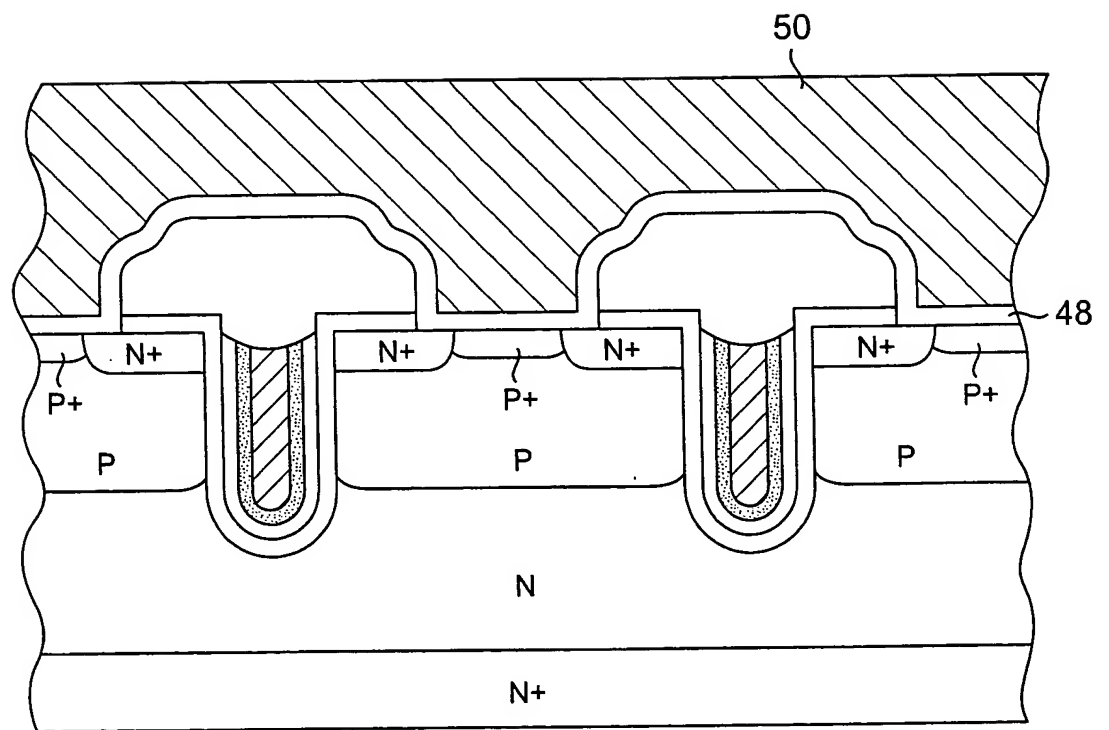


FIG. 2G

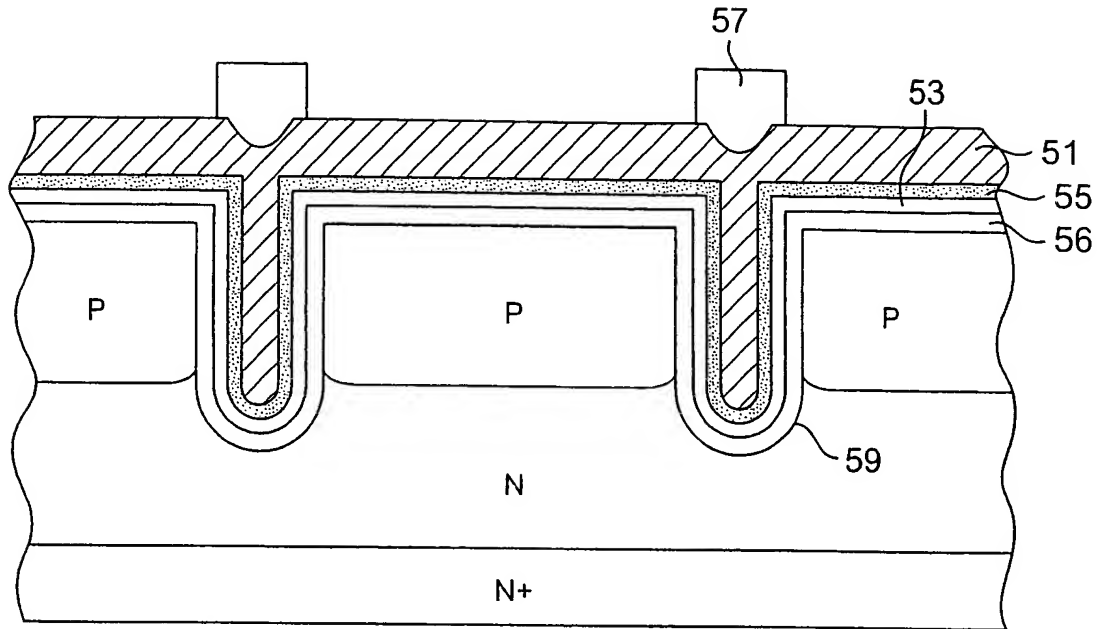


FIG. 3A

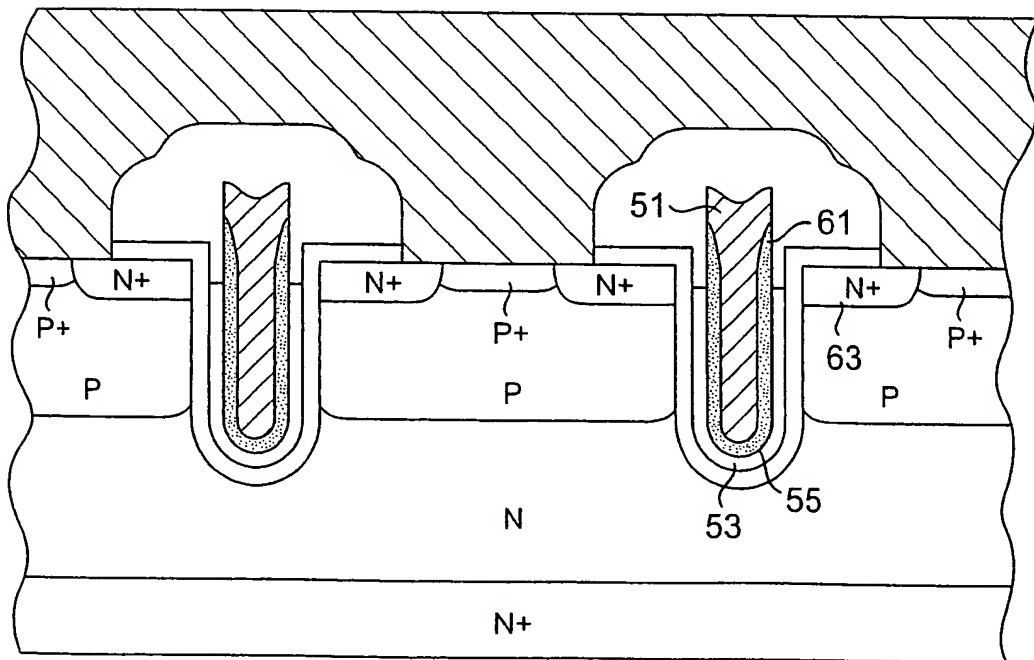


FIG. 3B

A cross-sectional diagram of a semiconductor device. The device consists of a substrate with a bottom layer labeled 'N+' and a middle layer labeled 'N'. Above the 'N' layer is a layer labeled 'P'. Two gate structures are formed on the 'P' layer. Each gate structure has a central channel region labeled 'N+' and is flanked by regions labeled 'P+'. The gate structures are labeled '65' and '69'. The channel regions are labeled '71'. The top of the device is covered by a layer with diagonal hatching.

FIG. 4B